

(SYLLABUS)

1.

(Course Title)		(Instructor)			
(Year)	2026	(Semester)	2	(Course No.)	2150152401
(Class)	01	(Open to)	2, 3, 4	(Course Classification)	-
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(Office)	704	(Telephone)	02-828-7489	(e-mail)	inchul.song@ssu.ac.kr
	(PBL)				
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
	Verilog-HDL, FPGA				
(Course Description)	FPGA				

(Digital Logic Circuit)	
Verilog HW verification	
FPGA targeting prototyping	

가	(100)	(100%)
	20	20
	30	30
	40	40
	10	10

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(Required Texts)		* / PPT
	()	* /Digital Design: With an introduction to the Verilog HDL, Vhdl, and Systemverilog/Mano, M. Morris / Ciletti, Mic/Pearson/2017/6th
	Vivado tool installation, Digilent Arty-S7 FPGA Board & USB cable, Pmod Dual 7-segment	
	3/4/6/7/9/10/11/12 14	

2.

(Week)	(Keyword)	(Description)		(Texts)
01		SW install		
02		AND/OR/XOR/NOT/NAND/NOR		
03	Multiplexer & De-multiplexer	Multiplexer De-multiplexer Verilog logic , FPGA targeting , Muxiplexer & De-multiplexer FPGA targeting		
04	Encoder & Decoder	Encoder decoder , Encoder & Decoder FPGA targeting		
05	Latch/Flipflop &	Latch FlipFlop , Latch & Flipflop FPGA targeting		
06	Register & Counter	Register Counter , Register & Counter FPGA targeting		
07	Adder/Multiplier & Accumulator	Adder/Multiplier accumulator , Adder/Multiplier & accumulator FPGA targeting		
08		(/)		
09	7-segment LED & Pmod interface	7-segment LED driver , Pmod interface , Chip to chip inteface , 7-segment driver FPGA targeting		
10		, / / FPGA targeting		
11	Stop watch/Timer	Stop watch timer , Stop watch & Timer FPGA targeting		
12	watch/Timer & Stop	Stop watch/Timer & Stop watch/timer FPGA targeting		

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13	(1/2)	Stop watch/Timer Alarm 가 , (Stop watch/Timer Alarm 가) (1/2)	, , ,	
14	(2/2)	Q&A, (Stop watch/Timer Alarm 가) (2/2)	, , ,	
15		(/)		

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3. ()

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	Open-ended problem		
	Teamwork		
	Communication skills		